

DESCRIPTION

The JW1386 is an integrated power solution for LCD Panel. JW1386 provides a boost converter for AVDD, positive charge pump for VGH, negative charge pump for VGL, gate pulse modulation function GPM and 1 channel operation amplifier for VCOM.

The JW1386 built in 0.2ohm NMOS with 3A current limit and 1MHz operation switching frequency. One channel positive charge pump for VGH, by internal voltage control and feedback control for stable output voltage. One channel negative charge pump for VGL by internal voltage control and feedback control for stable output voltage. It also provides gate pulse modulation for reducing flicker of panel and power on delay time can be set by external capacitor. Otherwise JW1386 provides one channel operation amplifier setting unity gain buffer for VCOM. And OP output can sink/source 200mA short circuit current. It built in voltage detect function for generating a reset signal during power on/off.

The device includes protection function such as under voltage lockout (UVLO) for input VDD, over voltage protection (OVP) for boost controller and under voltage protection (UVP) for each channel output voltage.

The JW1386 is available with 24 pin 4mm×4mm VQFN green packages.

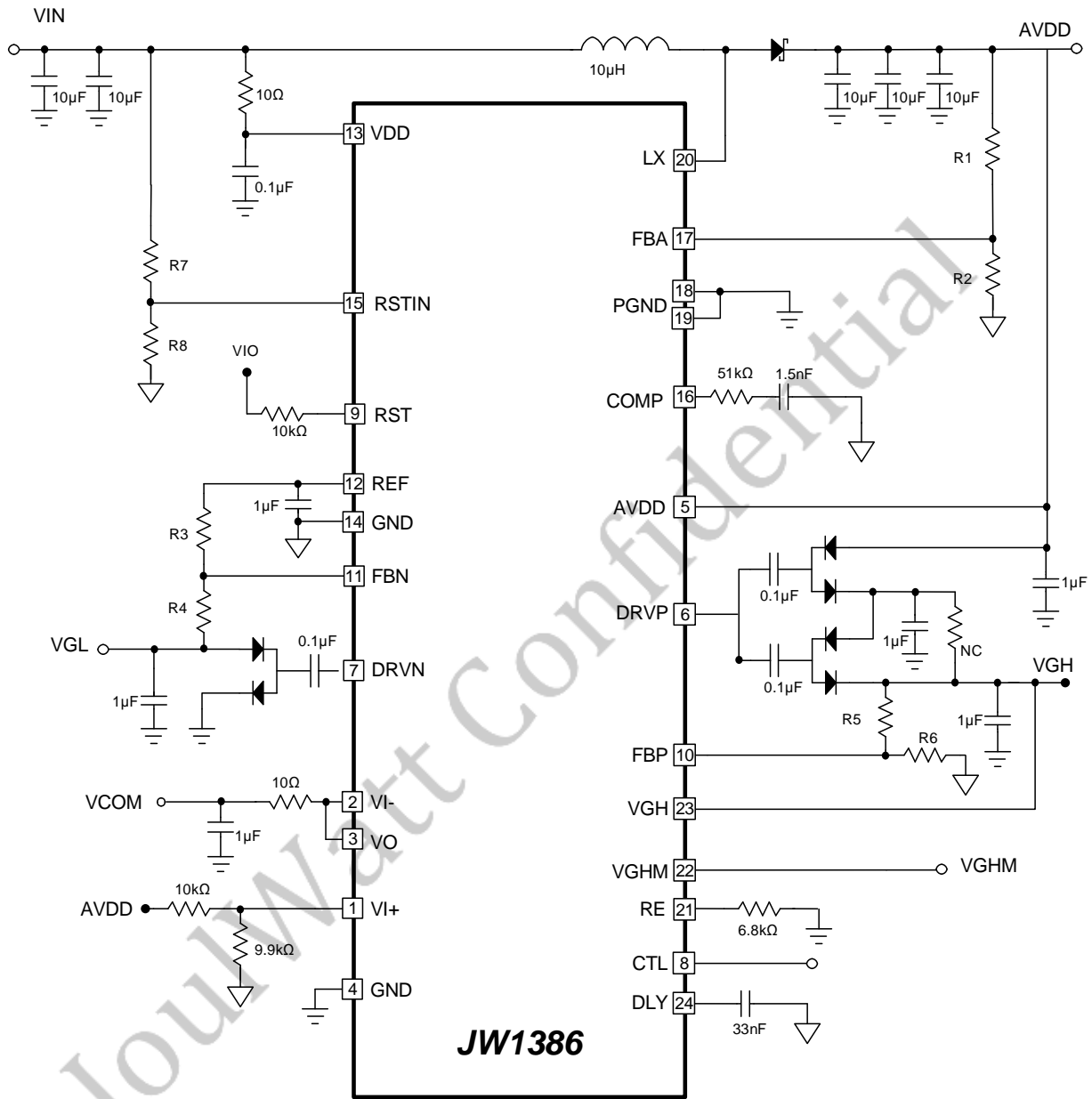
FEATURES

- 2.5V to 5.5V Input Voltage Range
- Boost Converter
 - Built in 20V, 3A, 0.2Ω Power MOS
 - 1MHz Switching Frequency
- Positive Charge Pump Regulator
- Negative Charge Pump Regulator
- Gate Pulse Modulation
 - Adjustable Power On Delay Time
- Operational Amplifier
 - ±200mA short circuit current
 - 35V/μs Slew Rate
- Voltage Detection
 - Open Drain Output
- Protection Function
 - Under Voltage Lockout (UVLO)
 - Over Voltage Protection (OVP)
 - Under Voltage Protection (UVP)
 - Over Temperature Protection (OTP)
- VQFN24 4X4mm Package Available

APPLICATIONS

- TFT-LCD GOA Panel

TYPICAL APPLICATION

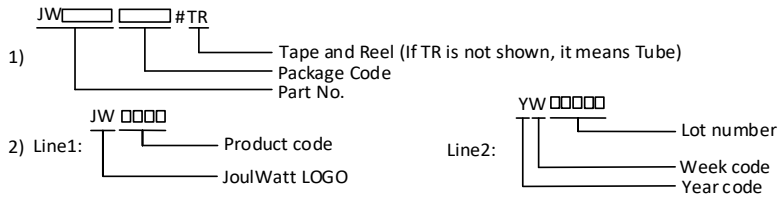


Application Schematic

ORDER INFORMATION

DEVICE ¹⁾	PACKAGE	TOP MARKING ²⁾	ENVIRONMENTAL ³⁾
JW1386VQDFA#TR	VQFN4x4-24	JW1386 YW□□□□	Green

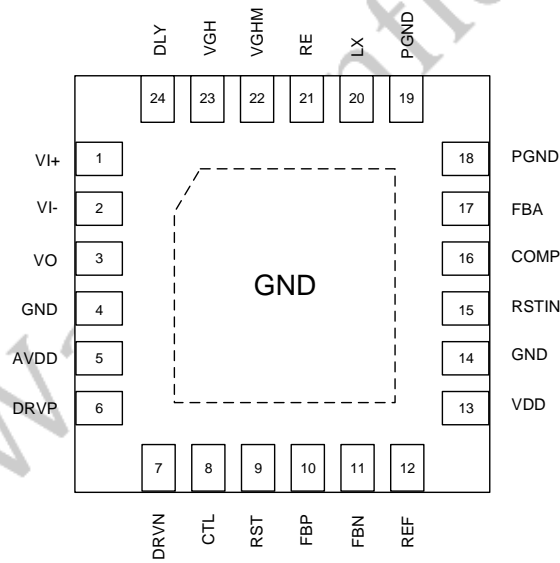
Notes:



3) All JoulWatt products are packaged with Pb-free and Halogen-free materials and compliant to RoHS standards.

PIN CONFIGURATION

TOP VIEW



ABSOLUTE MAXIMUM RATING¹⁾

VDD, RST to GND	-0.3V to +6.5V
AVDD, LX to GND	-0.3V to +20V
VGH, VGHM, RE to GND	-0.3V to +40V
FBA, FBP, FBN, CTL, RSTIN	-0.3V to VDD+0.3V
VI+, VI-	-0.3V to AVDD+0.3V
COMP, REF, DLY	-0.3V to VDD+0.3V
Junction Temperature ²⁾	-40°C to 150°C
Lead Temperature	260°C
Storage Temperature	-65°C to +150°C
ESD (HBM).....	±2kV
ESD (MM).....	± 200V

RECOMMENDED OPERATING CONDITIONS³⁾

Input Voltage VDD.....	3.3V to 5V
Output Voltage V _{GH}	15V to 38V
Output Voltage V _{GL}	-15V to -3V
Operating Junction Temperature	-40°C to 125°C

THERMAL PERFORMANCE⁴⁾

	θ_{JA}	θ_{JC}
VQFN4x4-24.....	45.6	7.5°C/W

Notes:

- 1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.
- 2) The JW1386 includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

VDD= 5V, VGH= 27V, VGL= -8V, VAVDD= 13V, Typical values are at TA = 25°C, unless otherwise specified.						
ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNITS
General						
VDD Input Range	VDD		2.5		5.5	V
AVDD Input Range	VAVDD		6		18	V
VDD UVLO Threshold	VDD_UVLO	Rising	2.15	2.25	2.35	V
		Falling	2.05	2.15	2.25	V
VDD Quiescent Current	IDD	LX Non Switching		0.5	1	mA
		LX Switching		1	3	mA
AVDD Operating Current	I _{AVDD}			1.5	5	mA
Thermal Shutdown Temperature	T _{ST}	Temperature Rising	130	150	170	°C
Reference Voltage						
Reference Voltage	V _{REF}		1.238	1.250	1.262	V
REF Line Regulation	LIR	IVREF=100μA, VDD=2.5V~5.5V		2	5	mV
REF Load Regulation	LOR	IVREF=0~100μA		1	5	mV
Boost Converter (AVDD)						
AVDD Output Range	VAVDD		6		18	V
Switching Frequency	Freq1 _{AVDD}		450	500	550	kHz
	Freq2 _{AVDD}		900	1000	1100	kHz
Maximum Duty	D _{AVDD}				95	%
FBA Feedback Voltage	V _{FBA}		1.238	1.25	1.262	V
FBA Bias Current	I _{FBA}				40	nA
Switching NMOS On Resistance	R _{ON}			200		mΩ
LX Leakage Current	I _{LX}	V _{LX} =18V		1	10	μA
Current Limit	I _{LIM}		3	3.5	4	A
FBA Under Voltage Protection Threshold	V _{FBAUVP}		0.95	1	1.05	V
FBA Under Voltage Protection Fault Time	T _{FBAUVP}		48	55	62	ms
FBA Short Circuit Protection Threshold	V _{FBASCP}			0.1		V
Over Voltage Protection Threshold	V _{OVP}		19.2	19.8	20.5	V
Over Voltage Protection Threshold Hysteresis	V _{HYP}		0.8	1	0.12	V
Soft Start Time	T _{SS}		10	11	12	ms

Negative Charge Pump Regulator (VGL)						
Input Supply Voltage Range	V _{INAVDD}		6		18	V
DRVN Switching Frequency	F _{DRVN}		450	500	550	kHz
DRVN High Side MOS On Resistance	R _{ONH}			3	6	Ω
DRVN Low Side MOS On Resistance	R _{ONL}			3	6	Ω
FBN Voltage Range	V _{FBN}		0.235	0.25	0.265	V
FBN Bias Current	I _{FBN}		-40		40	nA
FBN Under Voltage Protection Threshold	V _{FBNUV}		0.4	0.45	0.5	V
FBN Under Voltage Protection Fault Time	T _{FBNUV}		48	55	62	ms
Soft Start Time	T _{SS}		2.8	3.4	4	ms
Positive Charge Pump Regulator (VGH)						
Input Supply Voltage Range	V _{INAVDD}		6		18	V
Output Range	V _{GH}		15		38	V
DRVP Switching Frequency	F _{DRVP}		450	500	550	kHz
DRVP High Side MOS On Resistance	R _{ONH}			3	6	Ω
DRVP Low Side MOS On Resistance	R _{ONL}			3	6	Ω
FBP Voltage Range	V _{FBP}		1.23	1.25	1.27	V
FBP Bias Current	I _{FBP}		-40		40	nA
FBP Under Voltage Protection Threshold	V _{FBNUV}		0.95	1	1.05	V
Soft Start Time	T _{SS}		2.8	3.4	4	ms
Operation Amplifier (VCOM)						
Input Supply Voltage Range	V _{INAVDD}		6		18	V
Input Supply Current	I _{VIN}	V _{VI} ± AVDD/2			2	mA
Input Offset Voltage	V _{OFFSET}	V _{VI} ±5V		2	15	mV
Input Bias Current	I _{VI}	V _{VI} ±5V	-40		40	nA
Output Voltage Swing High	V _{OSH}	I _{VCOM} =20mA	AVDD-0.3			V
Output Voltage Swing Low	V _{OSL}	I _{VCOM} =20mA		0.2	0.3	V
Output Short Current	I _{OS+}			200		mA
	I _{OS-}			-200		mA
Slew Rate	SR	V _{VI} ±2V to 8V, 20% to 80% and 8V to 2V, and 80% to 20%	25	35		V/μs
Open Drain Output (RESET)						
RST Output Voltage	V _{RST}	I _{RST} =1.2mA		0.12	0.15	V
RSTIN Sense Voltage	V _{RSTIN}		1.23	1.25	1.27	V
RSTIN Hysteresis Voltage	V _{HYSRST}			50		mV
RSTIN Blanking Time	T _{BRST}			163		ms
RSTIN Input Bias Current	I _{BRST}		-40		40	nA

Gate Pulse Modulation (GPM)						
DLY Source Current	I _{DLY}		4	5	6	μA
DLY Threshold Voltage	V _{DLY}		1.2	1.25	1.3	V
DLY Discharge On Resistance	R _{DLY}				8	Ω
CTL Input High Voltage	V _{IH}				2	V
CTL Input Low Voltage	V _{IL}		0.5			V
CTL Input Bias Current	I _{BCTL}		-40		40	nA
Propagation Delay CTL to VGHM	T _{DLY}			100		ns
VGH to VGHM Switch On Resistance	R _{PON}			15		Ω
VGHM to Re Switch On Resistance	R _{NON}			30		Ω
VGHM to GND Pull Down Resistance	R _{PD}		1.5	2.5	3.5	kΩ

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PIN DESCRIPTION

Pin No.	Pin Name	I/O	Pin Function
1	VI+	I	OPA non Inverting input
2	VI-	I	OPA Inverting input
3	VO	O	OPA Output
4	GND		Ground of OPA and Charge Pump
5	AVDD	I	AVDD Power Supply for OPA and Charge Pump
6	DRVN	O	Positive Charge Pump Regulator
7	DRVP	O	Negative Charge Pump Regulator
8	CTL	I	Input Control Clock for VGHM
9	RST	O	RST Output Signal
10	FBP	I	Positive Charge Pump Feedback Pin
11	FBN	I	Negative Charge Pump Feedback Pin
12	REF	O	Reference Voltage
13	VDD	I	Main Power Supply Input
14	GND		Analog Ground
15	RSTIN	I	Comparator of RST Signal Input
16	COMP	O	Boost Error Amplifier Compensation Pin
17	FBA	I	Boost Converter Feedback Pin
18	PGND		Power Ground
19	PGND		Power Ground
20	LX	O	Boost Converter Switching Pin
21	RE	O	Gate Pulse Modulation Discharge Pin
22	VGHM	O	Gate Pulse Modulation Switching Output
23	VGH	I	High Voltage Supply for Gate Pulse Modulation
24	DLY	O	Delay time of Gate Pulse Modulation
25	E-PAD	P	Thermal Pad Need to Connect to Ground

BLOCK DIAGRAM

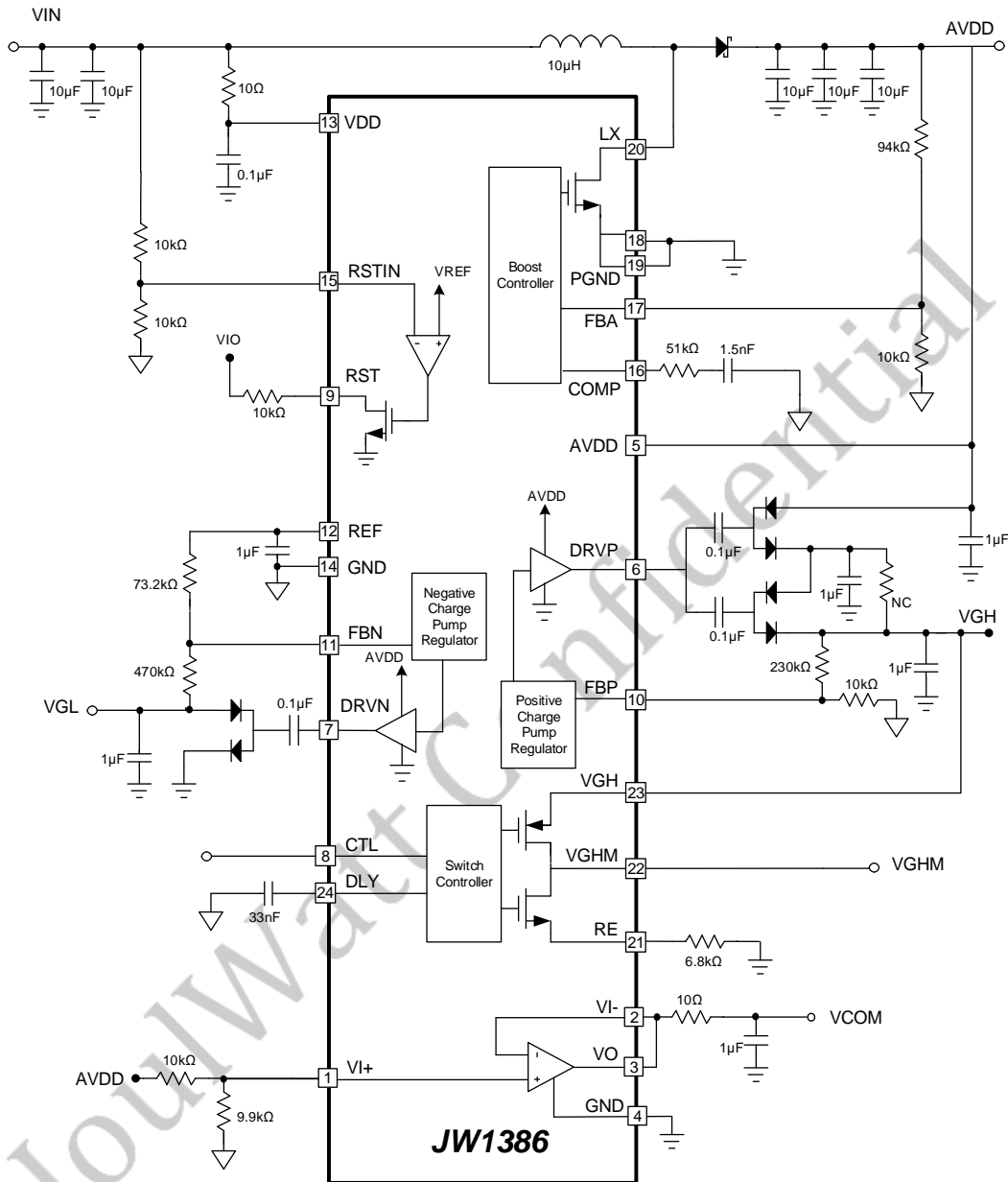


FIG1. JW1386 Function Block

POWER ON/OFF SEQUENCE

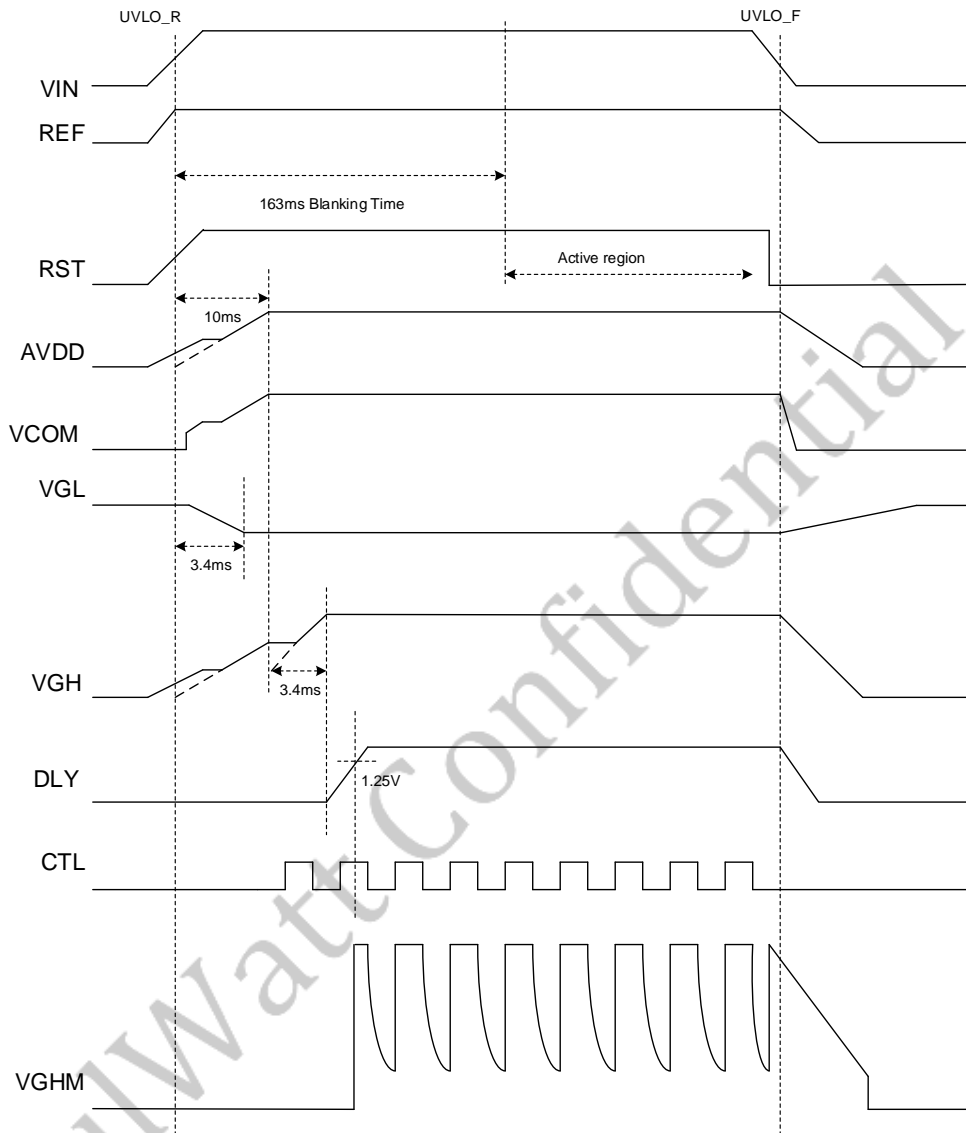


FIG. 2 Power ON/ OFF Sequence

FUNCTIONAL DESCRIPTION

Application Information

JW1386 provide multi power solution for TFT LCD panel. The device contains one channel boost converter for AVDD, one channel positive charge pump regulator for VGH and one channel negative charge pump regulator for VGL. The device also contains one channel operation amplifier for VCOM, gate pulse modulation for flicker compensation and voltage detect function with open drain structure for reset function.

In addition, the device includes various system protection schemes such as input under-voltage lockout (UVLO), output under voltage protection (UVP) and over temperature protection (OTP).

Boost Converter

Boost converter uses peak current mode PWM architecture, with 600k (option) / 1.2MHz (default) switching frequency. It have high efficiency and fast transient response. The input operating voltage of boost converter is 2.5V to 5.5V and output voltage is set by external resistor with FBA feedback control. By the way the maximum of output voltage is 18V, and over voltage protection is 19.6V (typ). The AVDD output can be calculated by following equation:

$$V_{AVDD} = 1.25V \times \left(1 + \frac{R1}{R2} \right)$$

Positive Charge Pump Regulator

The positive charge pump regulator provide high voltage for panel gate turn on. The structure of positive charge pump is determined by the number of stages. Output voltage is set by external resistor with FBP feedback control. The maximum of output voltage is 35V and the VGH output can be calculated by following equation:

$$V_{GH} = 1.25V \times \left(1 + \frac{R5}{R6} \right)$$

Negative Charge Pump Regulator

The negative charge pump regulator provide negative voltage for panel gate turn off. The structure of negative charge pump is determined by the number of stages. Output voltage is set by external resistor with FBN feedback control. The VGL output can be calculated by following equation:

$$V_{GL} = 0.25V - \frac{R4}{R3} (1.25V - 0.25V)$$

Operation Amplifier

The JW1386 includes one channel operation amplifier for VCOM function. The operation amplifier is capable of rail to rail input and output range and output with $\pm 200mA$ short circuit current. The operation amplifier can be designed in unity gain buffer configuration to generating VCOM voltage. The VO pin3 is the output of OP, it need to connect 10 ohm resistance and $1\mu F$ capacitance to ground for VCOM stable operation.

Gate Pulse Modulation

Gate Pulse Modulation is composed of two switch MOS between VGH to VGHM and VGHM to RE. GPM function is designed for flicker compensation, the purpose is to reduce coupling effect of gate line. The CTL pin is connected to external clock signal to determine the VGHM pull to VGH or discharge through RE. When CTL go high, high side switch will turn on, low side switch turn off and then VGHM pull to VGH voltage. If CTL go low, low side switch will turn on, high side switch turn off and then VGHM voltage discharge through RE to low level. During power off, VGHM

will pull high to VGH when VIN < UVLO or RST pull to low.

Reset Function

JW1386 have internal reset function with open drain structure. When power on, VIN exceed UVLO, RST have 163ms blanking time. During blanking time, RSTIN ignore the high/low signal and RST keeps in Hi_Z state. When the RSTIN voltage lower than the 1.25V (VREF), RST output will pull to low. The detect voltage can be calculated by following equation:

$$V_{DETECT} \times \frac{R8}{R7 + R8} = 1.25V = V_{RSTIN}$$

$$\text{Setting } V_{DETECT} > 1.25V \times \frac{R7 + R8}{R8}$$

For example:

If R7=R8=10k, 1.25V x (10k+10k)/10k =2.5V

We can set V_{DETECT}=VIN=5V

Thermal Protection

JW1386 provides thermal protection to prevent overheating in IC. When the junction temperature over Tj=160°C will trigger thermal sensor, it will shut down whole chip. It need to repower on to clear fault latch status then normal operating.

PCB Layout Note

For System performance such as stability, transient response, and EMI is greatly affected by the PCB layout. Below are some general layout guidelines as follow

1. Inductor

Always try to use shielded low EMI inductor with a ferrite core. The inductor should be placed as close to LX pin for reducing EMI, and the trace should be wide and short.

2. Bypass Capacitors

Place the low ESR ceramics bypass capacitors as close as possible to the VDD and VREF pins. This will help eliminate trace inductance effects and will minimize noise present on the internal supply rail. The ground connection of the VDD and VREF bypass capacitor should referenced to analog ground (GND).

3. Output Capacitors

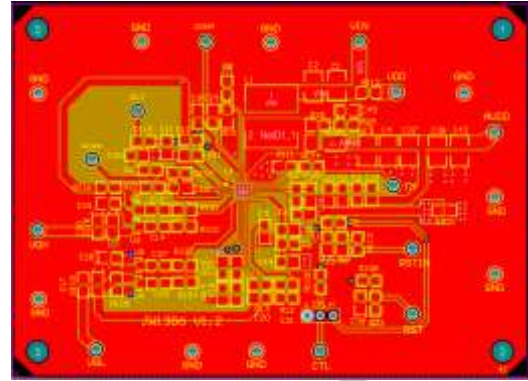
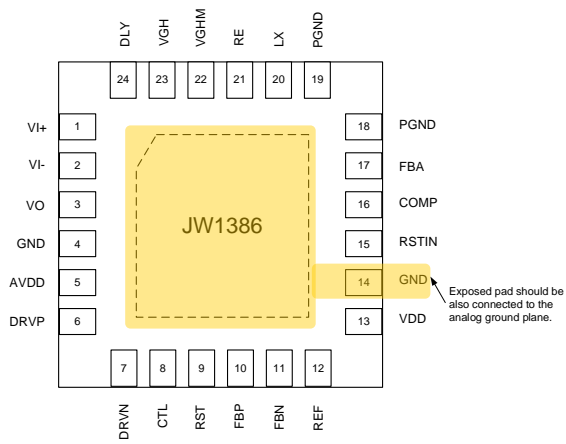
Minimize the trace length and maximize the trace width to minimize the parasitic inductance between the output capacitors of each regulator and its load for best transient response.

4. Feedback and Compensation Components

Any components for feedback, such as resistive divider networks for setting output voltage, should be placed as close as possible to its respective feedback pin. Minimize any feedback trace length to avoid noise. Likewise, compensation components should be place as close as possible to the pin.

5. Ground Plane

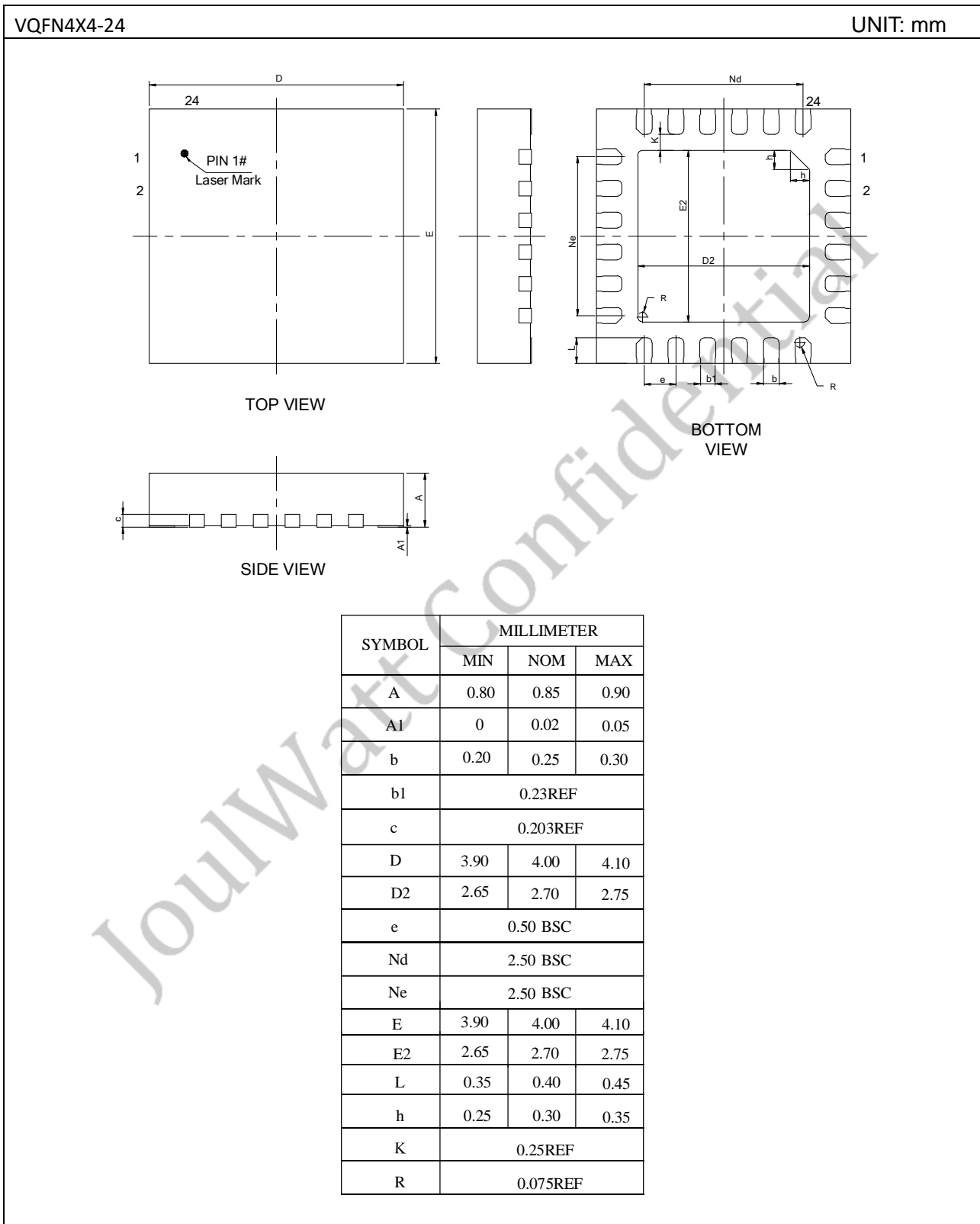
Use a power ground plane for the boost output capacitor ground, charge pump output capacitor grounds, and GND, PGND pins. All power ground nodes should be connected using short trace length but wide trace width, which helps to lower IR drop and minimize noise. Create an analog ground plane (GND) for VDD and VREF bypass capacitor grounds, compensation component ground, feedback resistive network grounds, DLY capacitor ground, RSTIN ground, and the GND pins also. Note that the IC's bottom side exposed pad should be also connected to the analog ground plane. Analog ground (GND) and power ground (PGND) should be connected only at one signal point, near the expose pad by shorting the GND pin to the expose pad.



6. Test Board for Reference
Top Layer

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PACKAGE OUTLINE



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